In the Claims:

1. (Original) A method of forming a silicon carbide MOSFET device having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3};

forming a p-type silicon carbide base region on the silicon carbide drift layer;

forming an n-type silicon carbide source region that defines a p-n rectifying junction with the p-type silicon carbide base region; and

forming a gate electrode on the p-type silicon carbide base region.

2. (Original) The method of Claim 1, wherein said step of forming a silicon carbide drift layer comprises annealing a boule-grown silicon carbide wafer at a sufficient temperature to reduce a trap density therein.

3. (Original) The method of Claim 2, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique or high-temperature CVD growth technique; and

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of silicon atoms to phosphorus atoms within the silicon carbide boule.

4. (Original) The method of Claim 1, wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

5. (Original) A method of forming a high-voltage silicon carbide device, comprising the steps of:

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3}; and

forming n-type and p-type silicon carbide layers on the silicon carbide drift layer.

6. (Original) The method of Claim 5, wherein said step of forming a silicon carbide drift layer comprises annealing a boule-grown silicon carbide wafer at a sufficient temperature to achieve a characteristic minority carrier lifetime in excess of 50 nanoseconds therein.

7. (Original) The method of Claim 6, wherein said step of forming a silicon carbide drift layer further comprises planarizing the silicon carbide wafer.

8. (Original) The method of Claim 6, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique or high-temperature CVD growth technique; and

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of silicon atoms to phosphorus atoms within the silicon carbide boule.

9. (Original) The method of Claim 5, wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

10. (Withdrawn) The method of Claim 6, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique or high-temperature CVD growth technique;

sawing the silicon carbide boule to yield a plurality of boule-grown silicon carbide wafers; and

irradiating the plurality of boule-grown silicon carbide wafers with thermal neutrons.

11. (Original) A method of forming a silicon carbide diode, comprising the steps of:

planarizing a boule-grown silicon carbide wafer having a net n-type dopant concentration therein, to define an n-type drift layer having opposing C and Si faces thereon and a thickness in a range from between about 100 μm and about 400 μm;

forming an n+ silicon carbide layer on the C-face of the n-type drift layer; and

forming a p+ silicon carbide layer on the Si-face of the n-type drift layer.

12. (Original) The method of Claim 11, wherein said planarizing step is preceded by the step of annealing the boule-grown silicon carbide wafer to reduce trap density therein.

13. (Original) The method of Claim 12, wherein said planarizing step is preceded by the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique or high-temperature CVD growth technique; and

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute silicon atoms in the silicon carbide boule into phosphorus atoms.

14. (Original) A method of forming a silicon carbide power device, comprising the step of:

planarizing a boule-grown silicon carbide wafer to define an n-type drift layer having opposing C and Si faces thereon and a thickness sufficient to support a blocking voltage in excess of 5kV.

15. (Original) The method of Claim 14, wherein said planarizing step is preceded by the step of annealing the boule-grown silicon carbide wafer to reduce trap density therein.

16. (Original) The method of Claim 15, wherein said planarizing step is preceded by the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique; and

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of the silicon atoms in the silicon carbide boule into phosphorus atoms.

17.-30. (Canceled)

31. (Original) A method of forming a high-voltage silicon carbide MOSFET device, comprising the steps of:

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3};

forming an n-type silicon carbide epilayer that extends on the silicon carbide drift layer and has a higher n-type dopant concentration therein relative to the silicon carbide drift layer;

forming a p-type silicon carbide base region that defines a p-n rectifying junction with the n-type silicon carbide epilayer;

forming an n-type silicon carbide source region that defines a p-n rectifying junction with the p-type silicon carbide base region; and

forming a gate electrode on the p-type silicon carbide base region.

32. (Original) A method of forming a silicon carbide JFET having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3};

forming an n-type silicon carbide epilayer on the silicon carbide drift layer;

forming an n-type silicon carbide source region in the n-type silicon carbide epilayer; and

forming a p-type silicon carbide gate electrode on the n-type silicon carbide epilayer.

33. (Original) The method of Claim 32, wherein said step of forming an n-type silicon carbide epilayer is preceded by the step of forming a p-type silicon carbide buried region in the silicon carbide drift layer; wherein said step of forming an n-type silicon carbide epilayer comprises forming an n-type silicon carbide epilayer that defines a p-n rectifying junction with the p-type silicon carbide buried region and a non-rectifying junction with the silicon carbide drift layer; and wherein said step of forming a p-type silicon carbide gate electrode comprises forming a p-type silicon carbide gate electrode that extends opposite a portion of the p-type silicon carbide buried region.

34. (Original) The method of Claim 33, further comprising the step of forming a source electrode that ohmically contacts the n-type silicon carbide source region and the p-type silicon carbide buried region.

35. (Original) The method of Claim 32, wherein said step of forming a silicon carbide drift layer comprises annealing a boule-grown silicon carbide wafer at a sufficiently high temperature to reduce a density of traps therein.

36. (Original) The method of Claim 32, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique; and

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute silicon atoms to phosphorus atoms within the silicon carbide boule.

37. (Original) The method of Claim 32, wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

38. (Original) A method of forming a silicon carbide MOSFET device having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a boule-grown silicon carbide drift layer having a net first conductivity type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3};

forming a second conductivity type silicon carbide base region on the silicon carbide drift layer;

forming a first conductivity type silicon carbide source region that defines a p-n rectifying junction with the second conductivity type silicon carbide base region; and

forming a gate electrode on the second conductivity type silicon carbide base region.

39. (Original) The method of Claim 38, wherein said step of forming a silicon carbide drift layer comprises annealing a boule-grown silicon carbide wafer at a sufficient temperature to reduce a trap density therein.

40. (Original) The method of Claim 39, wherein said step of forming a silicon carbide drift layer further comprises planarizing the silicon carbide wafer.

41. (Original) The method of Claim 38, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique; and

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of silicon atoms to phosphorus atoms within the silicon carbide boule.

42. (Original) The method of Claim 38, wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

43. (Canceled)

44. (Original) A method of forming a silicon carbide device having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3};

forming a p-type silicon carbide base region on the silicon carbide drift layer;

forming an n-type silicon carbide source region that defines a p-n rectifying junction with the p-type silicon carbide base region; and

forming a gate electrode on the p-type silicon carbide base region.

45. (Original) The method of Claim 44, wherein the device is selected from the group consisting of MOSFETs and IGBTs.